High Efficiency Thyristor

$V_{RRM} = 2 \times 1200$ V

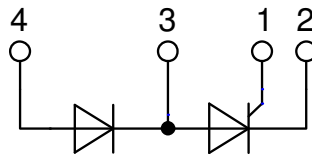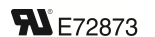$I_{TAV} = 100$ A

$V_T = 1,21$ V

Phase leg

Part number

CLA100PD1200NA

Backside: Isolated

E72873

Features / Advantages:
- Thyristor for line frequency
- Planar passivated chip
- Long-term stability

Applications:
- Line rectifying 50/60 Hz
- Softstart AC motor control
- DC Motor control
- Power converter
- AC power control
- Lighting and temperature control

Package: SOT-227B (minibloc)
- Isolation Voltage: 3000 V~
- Industry standard outline
- RoHS compliant
- Epoxy meets UL 94V-0
- Base plate: Copper internally DCB isolated
- Advanced power cycling

Terms -Conditions of usage:

The data contained in this product data sheet is exclusively intended for technically trained staff. The user will have to evaluate the suitability of the product for the intended application and the completeness of the product data with respect to his application. The specifications of our components may not be considered as an assurance of component characteristics. The information in the valid application- and assembly notes must be considered. Should you require product information in excess of the data given in this product data sheet or which concerns the specific application of your product, please contact the sales office, which is responsible for you.

Due to technical requirements our product may contain dangerous substances. For information on the types in question please contact the sales office, which is responsible for you.

Should you intend to use the product in aviation, in health or live endangering or life support applications, please notify. For any such application we urgently recommend
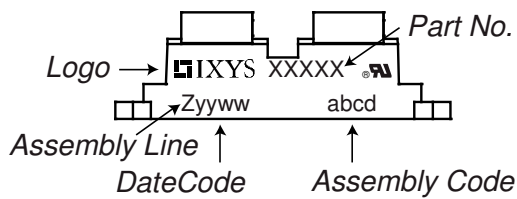- to perform joint risk and quality assessments;
- the conclusion of quality agreements;
- to establish joint measures of an ongoing product survey, and that we may make delivery dependent on the realization of any such measures.

IXYS reserves the right to change limits, conditions and dimensions.   Data according to IEC 60747and per semiconductor unless otherwise specified   20150827b

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CLA100PD1200NA

Rectifier

Symbol	Definition	Conditions		min.	typ.	max.	Unit
$V_{RSM/DSM}$	max. non-repetitive reverse/forward blocking voltage	T_{VJ} = 25°C				1300	V
$V_{RRM/DRM}$	max. repetitive reverse/forward blocking voltage	T_{VJ} = 25°C				1200	V
$I_{R/D}$	reverse current, drain current	$V_{R/D}$ = 1200 V	T_{VJ} = 25°C			50	µA
		$V_{R/D}$ = 1200 V	T_{VJ} = 125°C			2	mA
V_T	forward voltage drop	I_T = 100 A	T_{VJ} = 25°C			1,27	V
		I_T = 200 A				1,55	V
		I_T = 100 A	T_{VJ} = 125°C			1,21	V
		I_T = 200 A				1,58	V
I_{TAV}	average forward current	T_C = 85°C	T_{VJ} = 150°C			100	A
$I_{T(RMS)}$	RMS forward current	180° sine				150	A
V_{T0}	threshold voltage $\}$ for power loss calculation only		T_{VJ} = 150°C			0,83	V
r_T	slope resistance					3,7	mΩ
R_{thJC}	thermal resistance junction to case					0,35	K/W
R_{thCH}	thermal resistance case to heatsink				0,10		K/W
P_{tot}	total power dissipation	T_C = 25°C				350	W
I_{TSM}	max. forward surge current	t = 10 ms; (50 Hz), sine	T_{VJ} = 45°C			1,50	kA
		t = 8,3 ms; (60 Hz), sine	V_R = 0 V			1,62	kA
		t = 10 ms; (50 Hz), sine	T_{VJ} = 150°C			1,28	kA
		t = 8,3 ms; (60 Hz), sine	V_R = 0 V			1,38	kA
I^2t	value for fusing	t = 10 ms; (50 Hz), sine	T_{VJ} = 45°C			11,3	kA²s
		t = 8,3 ms; (60 Hz), sine	V_R = 0 V			10,9	kA²s
		t = 10 ms; (50 Hz), sine	T_{VJ} = 150°C			8,13	kA²s
		t = 8,3 ms; (60 Hz), sine	V_R = 0 V			7,87	kA²s
C_J	junction capacitance	V_R = 400 V f = 1 MHz	T_{VJ} = 25°C		77		pF
P_{GM}	max. gate power dissipation	t_P = 30 µs	T_C = 150°C			10	W
		t_P = 300 µs				5	W
P_{GAV}	average gate power dissipation					0,5	W
$(di/dt)_{cr}$	critical rate of rise of current	T_{VJ} = 150°C; f = 50 Hz repetitive, I_T = 300 A t_P = 200 µs; di_G/dt = 0,5 A/µs;				150	A/µs
		I_G = 0,5 A; V = ⅔ V_{DRM} non-repet., I_T = 100 A				500	A/µs
$(dv/dt)_{cr}$	critical rate of rise of voltage	V = ⅔ V_{DRM}	T_{VJ} = 150°C			1000	V/µs
		R_{GK} = ∞; method 1 (linear voltage rise)					
V_{GT}	gate trigger voltage	V_D = 6 V	T_{VJ} = 25°C			1,5	V
			T_{VJ} = -40°C			1,6	V
I_{GT}	gate trigger current	V_D = 6 V	T_{VJ} = 25°C			40	mA
			T_{VJ} = -40°C			80	mA
V_{GD}	gate non-trigger voltage	V_D = ⅔ V_{DRM}	T_{VJ} = 150°C			0,2	V
I_{GD}	gate non-trigger current					5	mA
I_L	latching current	t_p = 10 µs	T_{VJ} = 25°C			150	mA
		I_G = 0,5 A; di_G/dt = 0,5 A/µs					
I_H	holding current	V_D = 6 V R_{GK} = ∞	T_{VJ} = 25°C			100	mA
t_{gd}	gate controlled delay time	V_D = ½ V_{DRM}	T_{VJ} = 25°C			2	µs
		I_G = 0,5 A; di_G/dt = 0,5 A/µs					
t_q	turn-off time	V_R = 100 V; I_T = 100 A; V = ⅔ V_{DRM} T_{VJ} = 125 °C			150		µs
		di/dt = 10 A/µs dv/dt = 20 V/µs t_p = 200 µs					

Package	SOT-227B (minibloc)			Ratings			
Symbol	Definition	Conditions		min.	typ.	max.	Unit
I_{RMS}	RMS current	per terminal				150	A
T_{VJ}	virtual junction temperature			-40		150	°C
T_{op}	operation temperature			-40		125	°C
T_{stg}	storage temperature			-40		150	°C
Weight					30		g
M_D	mounting torque			1,1		1,5	Nm
M_T	terminal torque			1,1		1,5	Nm
$d_{Spp/App}$	creepage distance on surface | striking distance through air	terminal to terminal	10,5	3,2			mm
$d_{Spb/Apb}$		terminal to backside	8,6	6,8			mm
V_{ISOL}	isolation voltage	t = 1 second	50/60 Hz, RMS; I_{ISOL} ≤ 1 mA	3000			V
		t = 1 minute		2500			V

Product Marking

Logo →
Part No.
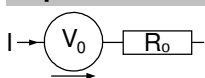Assembly Line ↑
DateCode
Assembly Code
Zyyww   abcd
IXYS XXXXX

Part description

C = Thyristor (SCR)
L = High Efficiency Thyristor
A = (up to 1200V)
100 = Current Rating [A]
PD = Phase leg
1200 = Reverse Voltage [V]
NA = SOT-227B (minibloc)

Ordering	Ordering Number	Marking on Product	Delivery Mode	Quantity	Code No.
Standard	CLA100PD1200NA	CLA100PD1200NA	Tube	10	509048

Similar Part	Package	Voltage class
CLA60PD1200NA	SOT-227B (minibloc)	1200

Equivalent Circuits for Simulation   *on die level T_{VJ} = 150 °C

Thyristor

$V_{0\,max}$	threshold voltage	0,83	V
$R_{0\,max}$	slope resistance *	1,8	mΩ

Outlines   SOT-227B (minibloc)

Dim.	Millimeter		Inches	
	min	max	min	max
A	31.50	31.88	1.240	1.255
B	7.80	8.20	0.307	0.323
C	4.09	4.29	0.161	0.169
D	4.09	4.29	0.161	0.169
E	4.09	4.29	0.161	0.169
F	14.91	15.11	0.587	0.595
G	30.12	30.30	1.186	1.193
H	37.80	38.23	1.488	1.505
J	11.68	12.22	0.460	0.481
K	8.92	9.60	0.351	0.378
L	0.74	0.84	0.029	0.033
M	12.50	13.10	0.492	0.516
N	25.15	25.42	0.990	1.001
O	1.95	2.13	0.077	0.084
P	4.95	6.20	0.195	0.244
Q	26.54	26.90	1.045	1.059
R	3.94	4.42	0.155	0.167
S	4.55	4.85	0.179	0.191
T	24.59	25.25	0.968	0.994
U	-0.05	0.10	-0.002	0.004
V	3.20	5.50	0.126	0.217
W	19.81	21.08	0.780	0.830
Z	2.50	2.70	0.098	0.106

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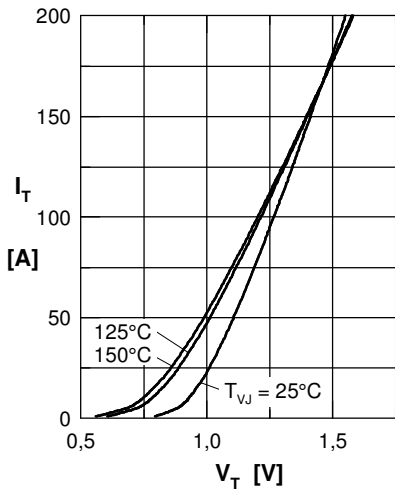**IXYS**

Thyristor

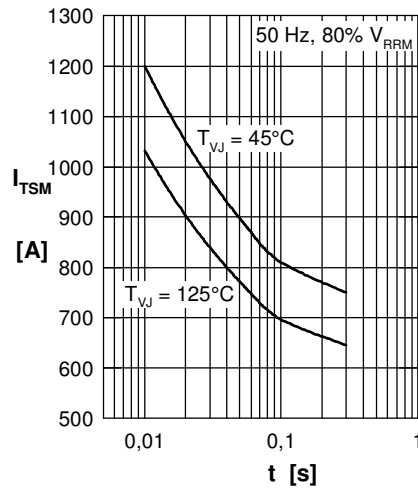Fig. 1 Forward characteristics

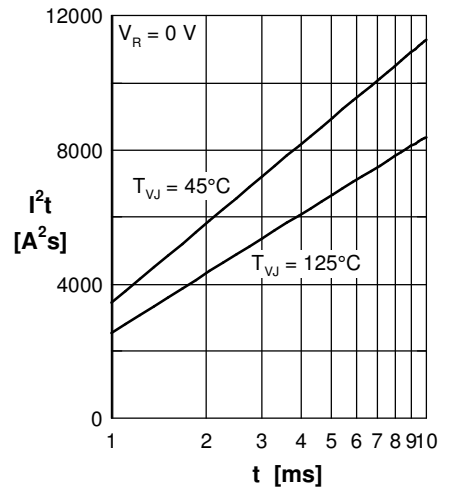Fig. 2 Surge overload current
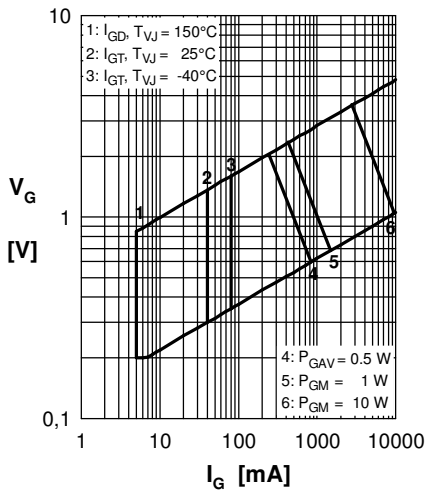

Fig. 3 I^2t versus time (1-10 ms)
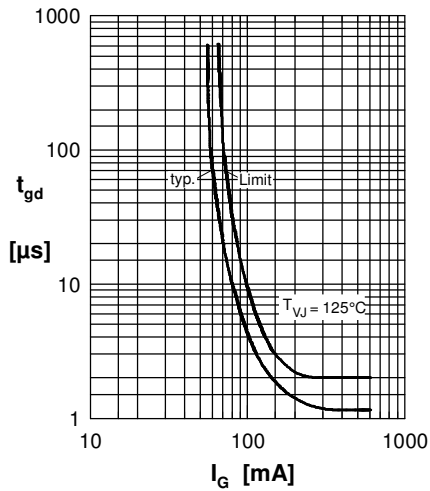

Fig. 4 Gate trigger characteristics

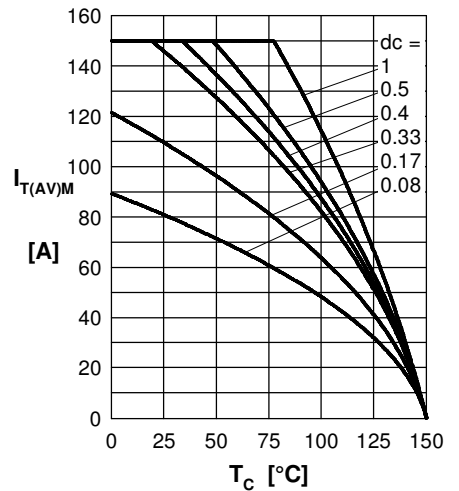Fig. 5 Gate controlled delay time

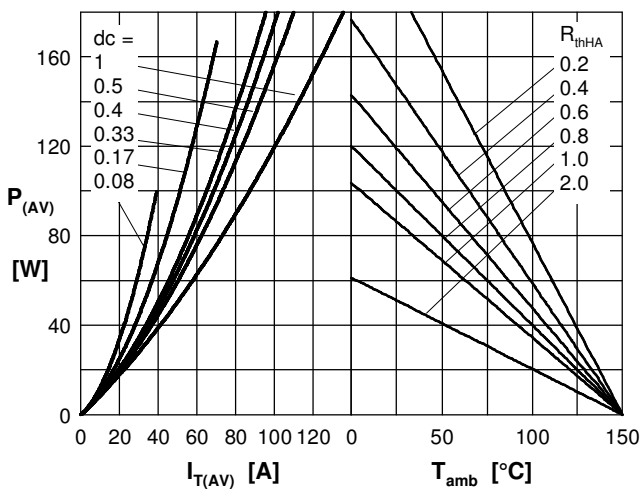Fig. 6 Max. forward current at case temperature

Fig. 7a Power dissipation versus direct output current
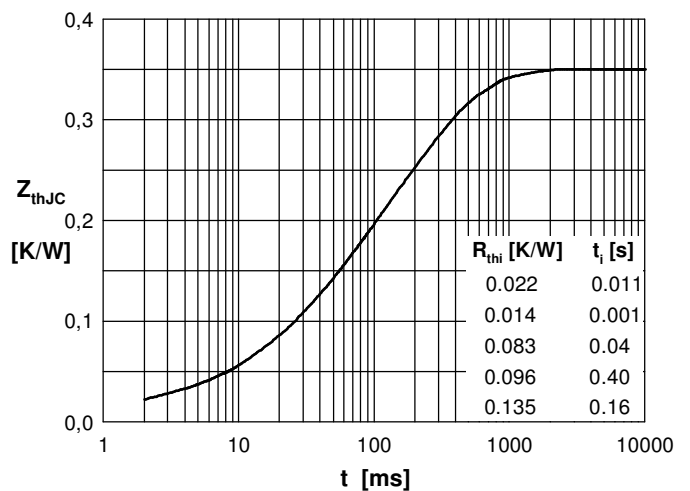Fig. 7b and ambient temperature

Fig. 8 Transient thermal impedance junction to case

R_{thi} [K/W]	t_i [s]
0.022	0.011
0.014	0.001
0.083	0.04
0.096	0.40
0.135	0.16